

REMARKS/ARGUMENTS

Claims 1-42 remain in the application. Of these, claims 28 and 36-42 stand allowed. Claims 7, 8, 10, 11, 17, 18, 20, 21, 23-26, 31, 32, 34 and 35 stand objected to as being dependent on rejected claims, but are otherwise allowable. Claims 1-6, 9, 12-16, 19, 22, 27, 29, 30 and 33 stand rejected.

Claims 12, 16, 33 and 36 have been amended to clarify that *control* of "P storage elements" comprises a *sequential enabling* of the P storage elements. Support for such an amendment is found, at least, in the paragraph beginning on page 31, line 20. As a result, the amendments to claims 12, 16, 33 and 36 are not believed to add new matter.

1. Rejection of Claims 1-6 & 9 Under 35 USC 102(b)

Claims 1-6 and 9 stand rejected under 35 USC 102(b) as being anticipated by CD4018B CMOS counter, TI Data Sheet, 1998.

Applicants' claim 1 recites "counter control logic" that 1) enables a counter "before each strobe signal is received", and 2) resets the counter "after each strobe signal is received". The Examiner asserts that such counter control logic is described by CD4018B in FIGS. 15 & 17 (wherein FIG. 15 shows the use of a PRESET input to enable a counter). Applicants respectfully disagree.

Although the counter described by CD4018B may be enabled and reset, CD4018B does not teach that enablement and reset of the counter are in any way tied to the counter's receipt of *each* of a number of strobe signals. Rather, it seems that the counter described by CD4018B merely updates a count in response to a *single, continuous clock signal*. In other words, although CD4018B's counter may be enabled and reset as desired, enablement and reset of the counter have no relation to starts, stops or changes in the clock signal received by the counter. Applicants' claim 1 is therefore believed to be allowable over the teachings of CD4018B in that CD4018B does not teach nor suggest counter control logic that enables and resets a

counter as recited in applicants' claim 1. Claims 2-4 are believed to be allowable over CD4018B at least for the reason that they depend from an allowable claim 1.

Applicants' claim 5 is believed to be allowable over CD4018B for reasons similar to those that make claim 1 allowable over CD4018B. That is, CD4018B does not teach nor suggest "counter control logic" that 1) enables a counter "*before each* strobe signal is received", and 2) resets the counter "*after each* strobe signal is received". Claims 6 and 9 are believed to be allowable over CD4018B at least for the reason that they depend from an allowable claim 5.

2. Rejection of Claims 1-6 & 9 Under 35 USC 102(a)

Claims 1-6 and 9 stand rejected under 35 USC 102(a) as being anticipated by Manning (U.S. Pat. No. 6,230,245).

Applicants' claim 1 recites "counter control logic" that 1) enables a counter "*before each* strobe signal is received", and 2) resets the counter "*after each* strobe signal is received". The Examiner asserts that such counter control logic is described by Manning in col. 2, lines 40-42. Applicants respectfully disagree.

As taught by Manning,

...the Counter 50 is an 8 stage quadrature counter which decrements from 255 to 0 responsive to the clock signals, CLK and clock CLK 90.

Manning, col. 5, lines 6-9.

Manning also teaches that CLK and CLK 90 are "generated by a conventional clock circuit 28" (col. 4, lines 11-13).

In light of Manning's above teachings, it is Applicants' position that Manning's counter is not enabled and disabled before/after receipt of each of a number of strobe signals. Rather, it seems that Manning's counter 50 receives a pair of continuously generated clock signals, but only decrements (i.e., counts) in response to the clock signals during periods when it is enabled to do so.

Applicants' claim 1 further recites that "counter control logic" resets a counter after each strobe signal is received by "receiving feedback from said counter". The Examiner asserts that such a reset based on counter "feedback" is taught by Manning in col. 5, lines 62-65. Applicants respectfully disagree.

As taught by Manning,

. . .At or before the terminal count, other circuitry in the integrated circuit causes the STOP signal to go active high, thereby causing the Counter Control circuit 46 to disable the Counter 50.

Manning, col. 5, lines 62-65.

Applicants believe it is too great a jump to conclude that the above statement supports resetting a counter based on feedback from the counter. Although Manning states that a STOP signal is caused to go active high "at or before the terminal count", Manning also states that it is "other circuitry in the integrated circuit" that causes the STOP signal to go active high. Manning does not state that the terminal count of the counter 50 is fed back to the "other circuitry". In fact, Manning says very little about how the "other circuitry" operates. Applicants therefore believe the Examiner is improperly using hindsight and their own teachings to read more into Manning than what Manning actually teaches.

For the above reasons, applicants' claim 1 is believed to be allowable over the teachings of Manning. Claims 2-4 are believed to be allowable over Manning at least for the reason that they depend from an allowable claim 1.

Applicants' claim 5 is believed to be allowable over Manning for reasons similar to those that make claim 1 allowable over Manning. That is, Manning does not teach nor suggest "counter control logic" that 1) enables a counter "before each strobe signal is received", and 2) resets the counter "after each strobe signal is received". Claims 6 and 9 are believed to be allowable over Manning at least for the reason that they depend from an allowable claim 5.

3. Rejection of Claims 12-16, 19, 22, 27, 29, 30 & 33 Under 35 USC 102(a)

Claims 12-16, 19, 22, 27, 29, 30 and 33 stand rejected under 35 USC 102(a) as being anticipated by Manning (U.S. Pat. No. 6,230,245).

The Examiner asserts that,

...Manning discloses memory controller receiver circuitry (Fig. 3), comprising: . . . b) P storage elements coupled to receive data from said data pad ($P \geq 2$), (Fig. 10 Ref. 190) said P storage elements being controlled by respective values of a count. . .

9/22/03 Office Action, p. 6, sec. 5.

Applicants respectfully disagree. If the Examiner equates the positions of Manning's Memory Array 190 with applicants' "P storage elements", then applicants believe the positions of Manning's Memory Array 190 are read and written under control of commands from Command Generator 26, and not under control of "respective values of a count". Although the Command Generator 26 generates different commands in response to different counts produced by a Counter 50 (Fig. 3), the value of a count produced by Counter 50 has no bearing on *which* of the positions in Memory Array 190 will be addressed. Rather, a count produced by Counter 50 only has a bearing on *if* some of the positions in Memory Array 190 will be addressed.

Applicants note that they have restated claim 12 to clarify how the recited "P storage elements" are "controlled by respective values of a count". That is, the P storage elements are "sequentially enabled to receive data by respective values of a count".

Applicants' claim 12 is believed to be allowable over the teachings of Manning for the above reason, and for reasons similar to those that make claim 1 allowable over Manning. Claims 13-15 are believed to be allowable over Manning at least for the reason that they depend from an allowable claim 12.

Applicants' claim 16 is believed to be allowable over Manning for reasons similar to those that make claim 12 allowable over Manning. Claims 19, 22 and 27

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are believed to be allowable over Manning at least for the reason that they depend from an allowable claim 16.

Applicants' claim 29 is believed to be allowable over Manning for reasons similar to those that make claim 1 allowable over Manning. Claim 30 is believed to be allowable over Manning at least for the reason that they depend from an allowable claim 29.

Applicants' claim 33 is believed to be allowable over Manning for reasons similar to those that make claim 12 allowable over Manning.

4. Conclusion

Given the above Remarks, applicants respectfully request that a timely Notice of Allowance be issued in this case.

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